

# Yang Zhao

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CONTACT INFORMATION	Department of Computer Science and Engineering University of California, Riverside Labs 465 Engineering Building II Riverside, CA 92521 USA	<i>E-mail:</i> zhaoy@cs.ucr.edu <i>WWW:</i> www.cs.ucr.edu/~zhaoy
CITIZENSHIP	China	
RESEARCH INTEREST	Formal methods on software/hardware verification Logic and probabilistic model checking Performance and dependability analysis	
QUALIFICATIONS	<b>Formal verification of software/hardware systems</b> Over 6 years research experiences and hand-on experiences on verifying real safety-critical systems (See “Work Experience”). Expertise on model checking. <b>C++/C, object-oriented programming</b> Over 8 years experiences on developing and debugging C++/C programs on Linux platform. Working as the main maintainer of the tool SMART. <b>Algorithm design and analysis</b> Published several papers proposing new symbolic algorithms to reduce the memory and runtime consumption in model checking and Markov Chain analysis (See “Academic Experience” and “Selected Publications”). <b>RTL design and verification</b> Over 2 years experiences of integrated circuit design and verification.	
EDUCATION	<b>University of California, Riverside, CA</b>  Ph.D. student, Computer Science, <b>expected graduation in July, 2013</b> <ul style="list-style-type: none"><li>• Advisor: Professor Gianfranco Ciardo</li><li>• Area of study: Software Engineering, Formal Verification</li></ul> <b>Institute of Computing Technology, CAS, Beijing, China</b>  M.S., Computer Science, July 2008 <ul style="list-style-type: none"><li>• Advisor: Professor Xiaowei Li</li><li>• Thesis: Formal Verification Techniques Based on Satisfiability</li></ul> <b>Peking University, Beijing, China</b>  B.S., Electrical Engineering, July 2005, minor in Mathematics	
ACADEMIC EXPERIENCE	<b>University of California, Riverside</b>  <i>Graduate Student Researcher</i>  Maintainer of the decision diagram library and verification tool SMART, designed and implemented new algorithms for: <ul style="list-style-type: none"><li>• Probabilistic model checking</li><li>• Steady-state solution for large continuous-time Markov Chain [QEST12]</li><li>• Shortest counterexample generation [TASE11]</li></ul>	<b>June 2009 to Now</b>

- Strongly connected component enumeration [NFM10][ISSE11]
- CTL model checking [ATVA09]

*Teaching Assistant* **September 2009 to December 2011**

- CS 008: Introduction to Computing
- CS 179K: Project in Computer Science: Software Engineering

**Institute of Computing Technology, CAS, Beijing, China**

*Research Assistant* **September 2005 to July 2008**

- Digital integrated circuit design and simulation-based verification

WORK  
EXPERIENCE

**NASA Ames Research Center, Moffett Field, CA**

*Intern Student* **June 2012 to August 2012**

*Advisor: Kristin Yvonne Rozier*

- Analyzed the dependability of NASA's next generation airspace control system using PRISM
- Produced quantitative results to guide the design decision
- Research paper in preparation

*Intern Student* **June 2011 to August 2011**

*Advisor: Kristin Yvonne Rozier*

- Verified NASA's next generation airspace control system using model checker NuSMV
- Found logic flaws in the original system designs that may lead to hazard
- Research paper presented in AVoCS 2012

**National Institute of Aerospace, Hampton, VA**

*Visiting Graduate Student* **June 2010 to September 2010**

*Advisor: Radu Siminiceanu*

- Integrated an MDD library written in C to the open-source model checker SAL, which is written in Scheme

**Ningbo IC Center, Ningbo, China**

*Development Assistant* **January 2008 to May 2008**

Design and verification of an embedded processor Low Power Processor (LPP)

AWARDS

UCR Dissertation Year Program Fellowship **Fall 2012**

QEST 2010 Student Travel Grant **September 2010**

UCR Dean's Distinguished University Fellowship **September 2008– June 2009**

TECHNICAL SKILLS

**Verification tools** SMART, NuSMV, PRISM, VIS, zChaff  
**Language** C++/C, Python, Java, Matlab, LISP, HTML/CSS, Verilog, SystemVerilog, E verification language  
**Tool** GNU make, autotools, Bison, gdb, gprof, Valgrind, SVN  
**IDE** Eclipse, Visual Studio  
**Operating Systems** Linux, Microsoft Windows, Apple OS X

**Yang Zhao** and Kristin Rozier, *Formal Specification and Verification of a Coordination Protocol for an Automated Air Traffic Control System*, International Workshop on Automated Verification of Critical Systems (AVoCS), 2012.

**Yang Zhao** and Gianfranco Ciardo, *A Two-Phase Gauss-Seidel Algorithm for Steady-state Solution of Structured CTMCs Encoded with EVMDDs*, International Conference on Quantitative Evaluation of Systems (QEST), 2012.

Gianfranco Ciardo, **Yang Zhao** and Xiaoqing Jin, *Ten Years of Saturation: A Petri Net Perspective*, Transactions on Petri Nets and Other Models of Concurrency V, pages 51-95, vol.6900, 2012.

Xiaoqing Jin, Gianfranco Ciardo, Tae-Hyong Kim and **Yang Zhao**, *Symbolic Verification and Test Generation for a Network of Communicating FSMs*, Automated Technology for Verification and Analysis (ATVA), 2011.

**Yang Zhao**, Xiaoqing Jin and Gianfranco Ciardo, *A Symbolic Algorithm for Shortest EG Witness Generation*, IEEE International Conference on Theoretical Aspects of Software Engineering (TASE), 2011.

**Yang Zhao** and Gianfranco Ciardo, *Symbolic Computation of Strongly Connected Components and Fair Cycles Using Saturation*, Innovations in Systems and Software Engineering, Volume 7, Number 2, Page 141-150, 2011.

**Yang Zhao** and Gianfranco Ciardo, *Symbolic Computation of Strongly Connected Components Using Saturation*, Second NASA Formal Methods Symposium (NFM), 2010.

Gianfranco Ciardo, **Yang Zhao** and Xiaoqing Jin, *Parallel symbolic state-space exploration is difficult, but what is the alternative?*, International Workshop on Parallel and Distributed Methods in Verification (PDMC), 2009.

**Yang Zhao** and Gianfranco Ciardo, *Symbolic CTL Model Checking of Asynchronous Systems Using Constrained Saturation*, Automated Technology for Verification and Analysis (ATVA), 2009.

**Yang Zhao**, Ling-yi Liu, Tao LV, Hua-wei Li and Xiao-wei Li, *Novel Circuit-Oriented SAT Engine and Its Application to Unbounded Model Checking* (poster in informal diguest), European Test Symposium (ETS), 2007.

Tao Lv, Tong Xu, **Yang Zhao**, Hua-wei Li and Xiao-wei Li, *Bug Analysis and Corresponding Error Models in Real Designs*, IEEE International High Level Design Validation and Test Workshop (HLDVT), 2007.

Tao Lv, Ling-yi Liu, **Yang Zhao**, Hua-wei Li and Xiao-wei Li, *An Observability Branch Coverage Metric Based on Dynamic Factored Use-Define Chains*, Asian Test Symposium (ATS), 2006.