Chen Tian

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BRIEF BIOGRAPHY

Chen Tian is a Staff System Researcher in Computer Science Lab at Samsung Information System America Inc., San Jose, California. His research interests span the areas of operating systems, runtime systems, compilers, programming languages, software engineering, and computer architectures. Particularly, he has been working on the following topics : operating system technologies for manycore processors; compiler and run-time system in resource constrained environments; compiling for speculative parallel execution; dynamic analysis for software reliability including debugging and failure-avoidance; architectural support for high performance computing.

Many research papers that Chen Tian authored or co-authored have been published in top-tier conferences and journals including Conference on Programming Language Design and Implementation (PLDI), International Symposium on Microarchitecture (MICRO), ACM Symposium on Principles and Practice of Parallel Programming (PPoPP), International Symposium on Software Testing and Analysis (ISSTA), and International Journal of Parallel Programming (IJPP). He also served as an external reviewer for many conferences and journals including PLDI, Transactions on Computers (TC) and Parallel Computing (Parco).

Chen Tian received his Ph.D. degree on Computer Science at the University of California at Riverside in June 2010. Before that he obtained his M.S. degree on Computer Science at the University of Arizona in 2007. He also obtained his M.S. degree on Mathematics at Beijing Jiaotong University in 2005.

EDUCATION

Ph.D. in Computer Science June 2010
The University of California at Riverside
Thesis title: Speculative Parallelization on Multicore Processors

M.S. in Computer Science May 2007
The University of Arizona

M.S. in Mathematics May 2005
Beijing Jiaotong University

B.S. in Mathematics May 2002
Beijing Jiaotong University

RESEARCH EXPERIENCE

Staff Researcher **Samsung Information Systems America Inc.** **July 2010 - Present**

Operating System Research for Manycore Processors
Role: System Architect and Lead Developer
We believe current monolithic kernel (e.g., Linux) has security and scalability issues due to its fundamental designs. We are currently developing a new highly scalable OS architecture based on L4 Microkernel technology. The key features of our system include scalable designs of most

OS components, resource control and security mechanisms as well as intelligent runtime system for energy and performance.

Compiler Research for Resource Constrained Environments
Role: Lead Developer
We are currently developing novel compiler, run-time technologies to support highly-efficient scaling in resource constrained multicore and manycore environments. A key emphasis of our work is the ability to support dynamic and adaptive scaling so that changes in resource availability (e.g., through different power-modes) and application load can be seamlessly managed from a Quality-of-Service (QoS) perspective. Our new solution also provides large-scale distributed computation coordination, live task migration, and adaptive scheduling. Project has been open sourced at *https://sourceforge.net/projects/snapple/* (accessible through invitation).

Research Assistant **University of Arizona and UC Riverside** **May 2006 - July 2010**

Compiling for Speculative Parallel Execution
The advent of multicores presents a promising opportunity for speeding up sequential programs via profile-based *speculative parallelization* of these programs. We propose the Copy or Discard (CorD) execution model to efficiently support software speculation on multicore processors.

Software Debugging, Failure-Avoidance
In multi-threaded programs, data race errors are very common and hard to detect. Having accurate synchronization information is crucial for detecting such errors. We present a dynamic *synchronization detection* technique that can effectively detect synchronizations and thus improve the accuracy of prior race detectors.

For programs that are multi-threaded and long-running, debugging them using trace based analysis is a very challenging problem due to the non-determinism and the exorbitant tracing overhead. We develop a novel scheme that using *logging/replay* and *execution reduction* techniques to address the challenges.

A large number of failures that occur in today's software, including those causing system crashes or producing wrong visible outputs, are due to the execution environment. These failures are often fixable by safe *execution perturbations* such as changing thread scheduling, padding memory allocations and dropping user requests. We present an on-line framework to capture and recover from failures by applying the perturbations and prevent them from occurring in the future.

PUBLICATIONS

COMPSAC	**C. Tian**, D. Waddinton and J. Kuang, "A Scalable Physical Memory Allocation Scheme For Microkernel", *IEEE Computer Software and Applications Conference, Industry Track*, Izmir, Turkey, July 2012.
TACO	M. Feng, **C. Tian**, C. Lin, M. Feng and R. Gupta, "Dynamic Access Distance Driven Cache Replacement", *ACM Transactions on Architecture and Code Optimization*, Volume 8 Issue 3, October 2011.
SP&E	D. Jeffrey, Y. Wang, **C. Tian**, and R. Gupta, "Isolating Bugs in Multithreaded Programs Using Execution Suppression", *Software: Practice and Experience*, Volume 41 Issue 11, October 2011.
PPoPP	**C. Tian**, C. Lin, M. Feng and R. Gupta, "Enhanced Speculative Parallelization Via Incremental Recovery", *16th ACM SIGPLAN Annual Symposium on Principles and Practice of Parallel Programming*, San Antonio, 2011. Acceptance Rate: **15% (26/165)**.
SFMA	D. Waddington, **C. Tian** and KC Sivaramakrishnan "Scalable Lightweight Task Management for MIMD Processor", *Systems for Future Multicore Architectures*, Salzburg, Austria, 2011.

PLDI	**C. Tian**, M. Feng and R. Gupta, "Supporting Speculative Parallelization In The Presence Of Dynamic Data Structures", *ACM SIGPLAN 2010 Conference on Programming Language Design and Implementation*, Toronto, Canada, 2010. Acceptance Rate: **20% (41/204)**.
SP&E	D. Jeffrey, Y. Wang, **C. Tian** and R. Gupta, " Isolating Bugs in Multithreaded Programs Using Execution Suppression", *Software: Practice and Experience*, accepted October 2010.
IJPP	**C. Tian**, M. Feng, V. Nagarajan and R. Gupta, "Speculative Parallelization of Sequential Loops On Multicores", *International Journal of Parallel Programming*, Volume 37, Issue 5, Page 508, 2009.
SP&E	**C. Tian**, V. Nagarajan, R. Gupta and S. Tallam, "Automated dynamic detection of busy-wait synchronizations", *Software: Practice and Experience*, Volume 39, Issue 11, Page 947, 2009.
ISMM	**C. Tian**, M. Feng and R. Gupta, "Speculative Parallelization Using State Separation and Multiple Value Prediction", *International Symposium on Memory Management*, Toronto, Canada, 2010. Acceptance Rate: **43% (13/30)**.
MICRO	**C. Tian**, M. Feng, V. Nagarajan and R. Gupta, "Copy Or Discard Execution Model For Speculative Parallelization On Multicores", *IEEE/ACM 41th International Symposium on Microarchitecture*, Lake Como, Italy, 2008. Acceptance Rate: **19% (40/210)**.
ICSM	S. Tallam, **C. Tian**, and R. Gupta, "Dynamic Slicing of Multithreaded Programs for Race Detection", *International Conference on Software Maintenance.*, Beijing, China, 2008. Acceptance Rate : **25 % (40/156)**.
ISSTA	**C. Tian**, V. Nagarajan, R. Gupta, and S. Tallam, "Dynamic Recognition of Synchronization Operations for Improved Data Race Detection", *International Symposium on Software Testing and Analysis.*, Seattle, 2008. Acceptance Rate : **26% (26/100)**.
COMPSAC	S. Tallam, **C. Tian**, X. Zhang, and R. Gupta, "Avoiding Program Failures through Safe Execution Perturbations", *IEEE Computer Software and Applications Conference.*, Turku, Finland, 2008. Acceptance Rate : **20%**.
STMCS	**C. Tian**, V. Nagarajan and R. Gupta, "Synchronization Aware Conflict Resolution for Runtime Monitoring Using Transactional Memory", *Workshop on Software Tools for Multicore Systems*, Boston, 2008.
NSFNGS	R. Gupta, N. Gupta, X. Zhang, D. Jeffrey, V. Nagarajan, S. Tallam and **C. Tian** "Scalable Dynamic Information Flow Tracking and its Applications", *NSF Next Generation Software Workshop*, Florida, 2008.
ISSTA	S. Tallam, **C. Tian**, X. Zhang, and R. Gupta, "Enabling Tracing of Long-Running Multithreaded Programs via Dynamic Execution Reduction", *International Symposium on Software Testing and Analysis*, London, UK, 2007. Acceptance Rate : **22% (22/101)**.

BOOK CHAPTER

- Chapter "Software Based Speculative Parallelization For Multicore/Manycore Architecture" has been accepted in book *Programming Multi-core and Many-core Computing Systems*, to be published in 2012.

PATENTS

- Scalable, Customizable and Load-balancing Physical Memory Allocator, US Patent Application #13/411,148, 2012.
- Coupled Lock Allocation and Lookup for Shared Data Synchronization in Symmetric Multithreading Environments, US Patent Application #13/408,163, 2012.
- Prevention of Race Conditions in Library Code Through Memory Page-fault Handling Mechanisms, US Patent Application #13/425,312, 2012.
- NUMA Aware System Task Management, US Patent Application #13/077,612, 2011.
- Adaptive Queuing Methodology For System Management, US Patent Application #13/077,567, 2011 .

PROFESSIONAL ACTIVITIES

- Member of Association for Computing Machinery (**ACM**).
- Member of Institute of Electrical and Electronics Engineers (**IEEE**).
- Reviewed papers for conferences, journals and books:
  IEEE Transactions on Computers 2013
  The conference on Languages, Compilers and Tools for Embedded Systems 2013
  ACM Transactions on Architecture and Code Optimization 2013
  IEEE International Parallel and Distributed Processing Symposium 2013
  IEEE International Symposium on Software Reliability Engineering 2012
  Parallel Computing 2012
  IEEE Computer Architecture Letters, 2011
  IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011
  Parallel Computing 2011
  Wiley book *Programming Multi-core and Many-core Computing Systems*, 2011
  Conference on Programming Language Design and Implementation 2011
  IEEE Transactions on Computers 2011
  Science of Computer Programming 2011
  Conference on Programming Language Design and Implementation 2010
  IEEE Transactions on Computers 2010
  Parallel Computing 2010
  ChinaCom 2007
  Parallel Computing 2007
  Parallel Computing 2006

SKILL SET

- Language: **C**, **C++**, **(GCC Inline) Assembly**.
- OS: **L4/Fiasco.OC**, **L4RE**, **Genode OS**, **L4/Pistachio**, **Linux**.
- Instrumentation Tools: **Pin**, **Valgrind**.
- Simulators: **SESC**, **Simics**.
- Compilers: **ROSE**, **LLVM**.
- Other skills obtained from earlier projects or prior working experience:
  Perl, **Java**, **Javascript/JQuery**, **MySQL**, **TCP/IP**, **JSP**.