Jia Yu

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Research Areas/Interests

Network processors and their compilers; Low power CPU design; Modeling, simulation and verification

Education

- **Ph.D.** in Computer Science, University of California, Riverside, 2002 to present, Exp. June 07
  Advisor: Jun Yang, Laxmi Bhuyan
  Thesis: High Performance and Low Power Network Processor Design
- **M.Sc** in Computer Science, University of California, Riverside, Dec. 2004
- **S.M.** in Computer Science, Singapore-MIT Alliance, University of California, Riverside, June 2002
- **B.Eng.** in Computer Science and Engineering, Zhejiang University, PRC, June 2000

Publication

- Jia Yu, Jinnan Yao, Laxmi Bhuyan, Jun Yang, "Program Mapping onto Network Processors by Recursive Bipartitioning and Refining", to appear in *44th Design Automation Conference(DAC)*, 2007
- Yan Luo, Jia Yu, Jun Yang, Laxmi Bhuyan, "Conserving Network Processor Power Consumption By Exploiting Traffic Variability," accepted by *ACM Transactions on Architecture and Code Optimization (TACO)*, 2006
- Jia Yu, Jun Yang, Shaojie Chen, Yan Luo, Laxmi Bhuyan, "Enhancing Network processor Simulation Speed With Statistical Input Sampling," *International Conference on High Performance Embedded Architectures & Compilers (HiPEAC)*, 2005
- Yan Luo, Jia Yu, Jun Yang, Laxmi Bhuyan, "Low Power Network Processor Design using Clock Gating", *42th Design Automation Conference(DAC)*, 2005
- Jia Yu, Wei Wu, Xi Chen, Harry Hsieh, Jun Yang, F. Balarin, "Assertion-Based Automatic Design Exploration of DVS in Network Processor Architectures", *Design, Automation and Test in Europe(DATE)*, 2005
- Jun Yang, Jia Yu, and Youtao Zhang, "A Low Energy Cache Design for Multimedia Applications Exploiting Set Access Locality," *Journal of Systems Architecture (JSA)*, Vol. 51, No. 10-11, October-November 2005
- Jia Yu, Wei Wu, Xi Chen, Harry Hsieh, Jun Yang, F. Balarin, "Assertion-Based Power/Performance Analysis of Network Processor Architecture", *International Workshop on High Level Design Validation and Test(HLDVT)*, 2004
- Jun Yang, Jia Yu, Youtao Zhang, "Lightweight Set Buffer: Low Power Data Cache for Multimedia Applications", *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, 2003
- Luying Zhou, Bei Yu, Jia Yu, "Light Path Protection for IP/DWDM Networks", *International Conference on Optical Communications and Networks (ICOCN)*, 2002

Experience

- ***University of California, Riverside, 2002-present*** – Research Assistant
  NePSim project: Participated in the development of the first open-source cycle-accurate execution-driven simulator of Intel IXP1200/2xxx network processor (NP). NePSim simulates a multi-core multi-threading NP with power evaluation framework.
  Source code available from *http://www.cs.ucr.edu/~yluo/nepsim/*, ***3530 web page visits and 806 downloads until Sept 2006***
  Technical highlights: cycle-accurate execution driven simulation, power modeling, benchmarking, verification, Intel IXA SDK.

Power-efficient network processors: With NePSim, we applied state-of-art power saving techniques such as Dynamic Voltage Scaling to reduce power dissipation. Developed a low-power scheme to power down idle cores during low workload.
Program mapping on network processors: Designed program mapping algorithms for parallel pipelined multi-core architecture. The average throughput improvement is around 20%, verified using SUIF/Machine SUIF and Intel IXA Architecture tool.
Enhancing network processor simulation speed: Applied statistical sampling method to accelerate network processor simulations by 10+ times.
Low power cache design: Designed a scheme to buffer and accessing the last accessed cache set instead of driving the tag and data banks, when applications show good set locality.
Trace cache and trace predictor: Designed frequent loop trace cache and trace predictor in Simplescalar 3.0.

- ***Intel Microprocessor Technology Lab, Santa Clara, summer 2006*** - Graduate Research Intern
  Studied performance of cache coherence protocol and L2 cache in multi-core architecture using SoftSDV full system simulator. Developed a module to model cache behavior in SoftSDV.

- ***Synopsys, PRC, winter 2004*** – Graduate Intern
  Wrote VHDL and Verilog testing programs for Synopsys Scirocco toolset, and used interactive debugger to identify the problems.

- ***Institute for Infocomm Research, Singapore, 01/2002 -06/2002*** – Research Assistant
  Designed and evaluated routing algorithms that improve path protection and quality of service in IP/DWDM optical networks.

- ***Microsoft, PRC, 07/ 2000-07/2001 –*** Windows Support Engineer
  Provided technical support for Windows Me, Windows 2000, and .NET release. Helped enterprise customers to set up Windows domain server.

- ***Zhejiang University, PRC, 1998-2000 –*** Research Assistant
  Studied the performance of rule-based expert system used in network intrusion detection software.

Teaching (Teaching Assistant in UC Riverside)

- **Discrete Mathematics** in Fall 2006; **Computer Architecture** for two quarters in 2004; **Design and Architecture of Computer Systems** in Summer 2004; **Computer Network** in Fall 2003; **Compiler Design** for three quarters in 2003, 2004; **Introduction to Computer Science** in 2003; **Concurrent Programming and Parallel Systems** in Fall 2002

Relevant Skills

- Intel IXA SDK and Architecture Toolset, SoftSDV, Pthread, MPI
- C/C++, JAVA, Perl, Bash, Python, MIPS, x86
- HDL (Verilog and VHDL)
- Cadence design tool, Synopsys Scirocco, Synopsys design compiler, Aldec HDL environment, Wind River Tornado

Selected Academic Projects

System and Network

- Designed and implemented dynamic replica selection in the **Globus data Grid**. The replica was chosen based on current and forecasted grid status.
- Implemented client/server file sharing protocol using Socket programming in Linux.
- Implemented routing algorithm simulation for large network on an eight-node cluster using MPI.

Compiler

- **Decaf compiler**: member of a 4-people group constructing front-end and back-end of Decaf compiler. Completed five segments including scanner and parser, semantic checker, code generator, data-flow optimizer, and instruction optimizer.
- **Front-end of MiniJava compiler**: implemented scanner, parser, symbol table, and abstract syntax tree for MiniJava without using Lex, Yacc tool. The code was published as reference solution to students in an

undergraduate compiler course. Source code link: http://www.cs.jhu.edu/~phf/2003/winter/cs152/downloads.html

- **Control and data dependency analysis for network applications:** developed a program dependency graph pass in Machine SUIF compiler tool. The results were used in program mapping for network processors.

VLSI

- Completed the schematics and layout of 4-bit adder, SRAM memory cell, 4-bit SRAM shift register, and FPGA configurable logic block (CLB) using **Cadence CAD design tools**.
- Completed the schematic of 32-bit ALU, and estimated its dynamic power consumption using 0.25uM technology in **Cadence Virtuoso Spectre Simulator**.

Honors

- Dean's Fellowship, Research Scholarship, UC Riverside, 2002-present
- Research Scholarship, MIT summer camp, NUS, MIT, 2001-2002
- MCSE, MCP, MCP+I certification, Microsoft service camp, Microsoft, 2000
- "Excellent Undergraduate Student", "All round excellent student", "Procter & Gamble Scholarship", awarded to 10% undergraduate students. ZJU 1997-2000

References

Available upon request