UC RIVERSIDE UNIVERSITY OF CALIFORNIA


# Multi-terminal PCB Escape Routing for Digital Microfluidic Biochips using Negotiated Congestion

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# Outline

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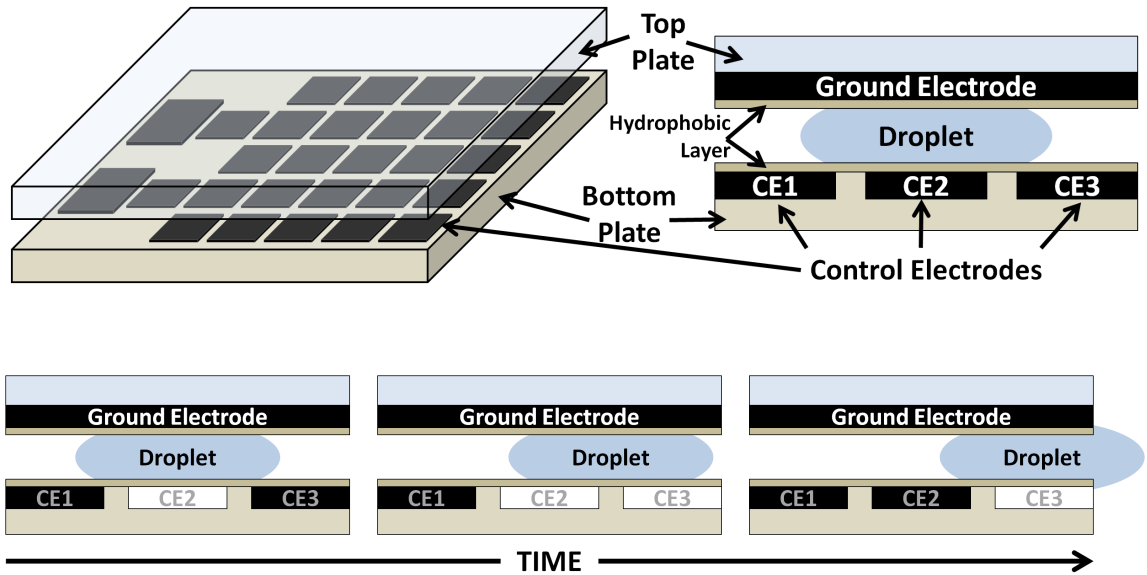
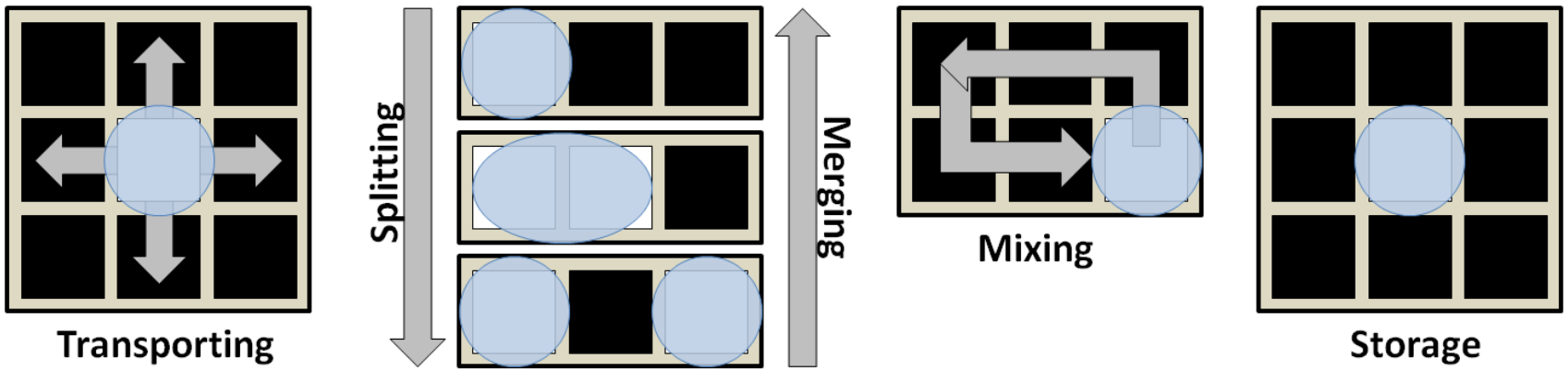
# Digital Microfluidics



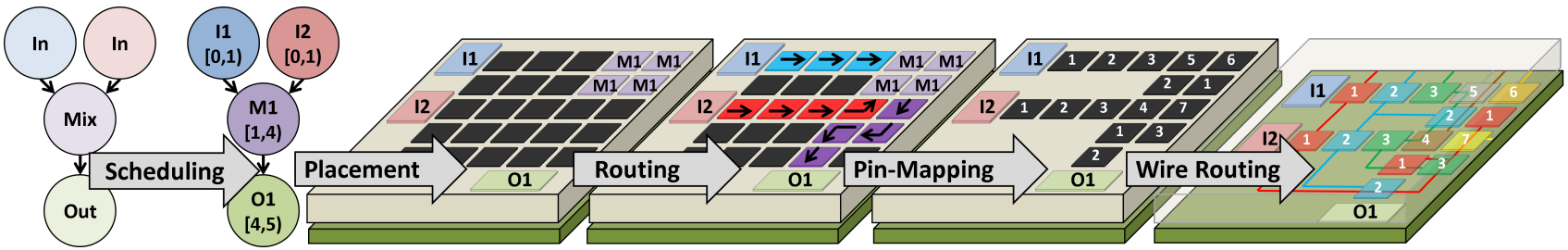

- Discrete droplets are moved around a 2D array of electrodes

# Basic Operations




- Five basic operations are combined to perform biology and chemistry experiments (assay)

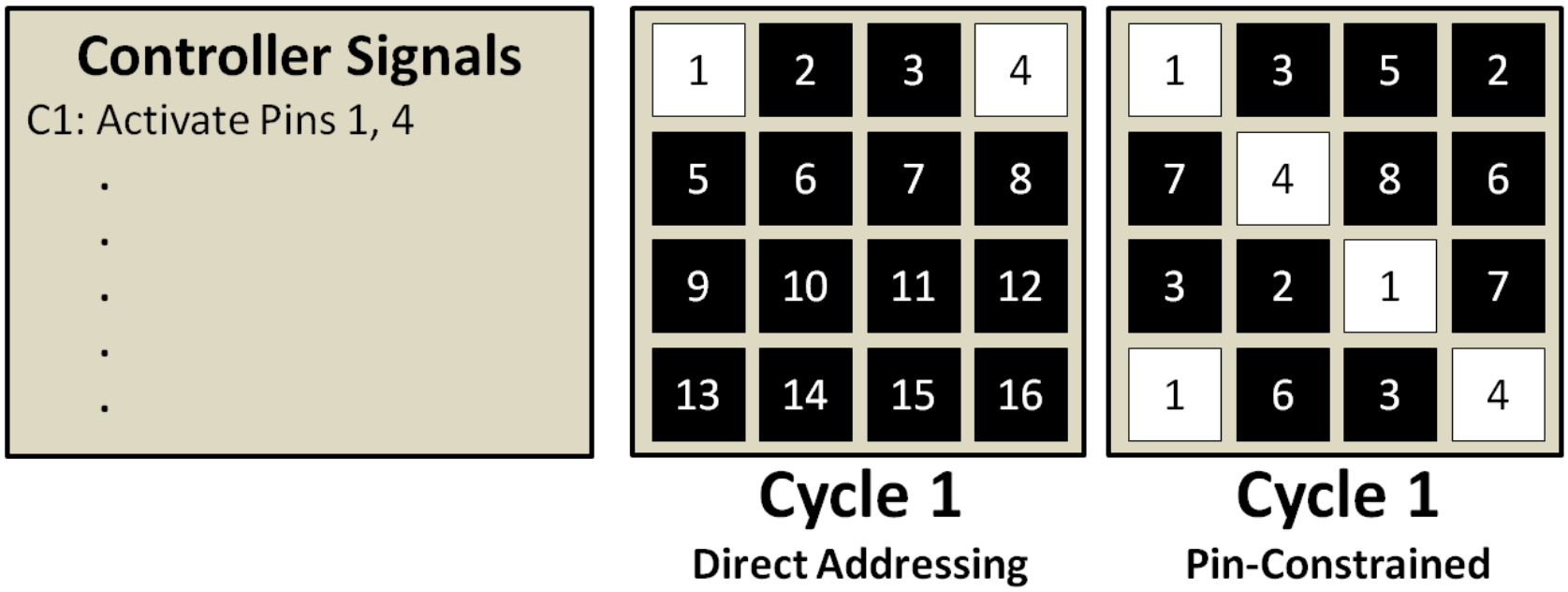
# Synthesis process




1. Schedule operations of the experiment, or assay
2. Place the components on to the DMFB array
3. Route the fluids between the components to perform the necessary operations
4. Perfrom the pin mapping of electrodes to external control pins
5. Route the wires on the PCB

# Pin Mapping

- Direct addressing: external control pin for each electrode
- Pin constrained: multiple electrodes share a control pin



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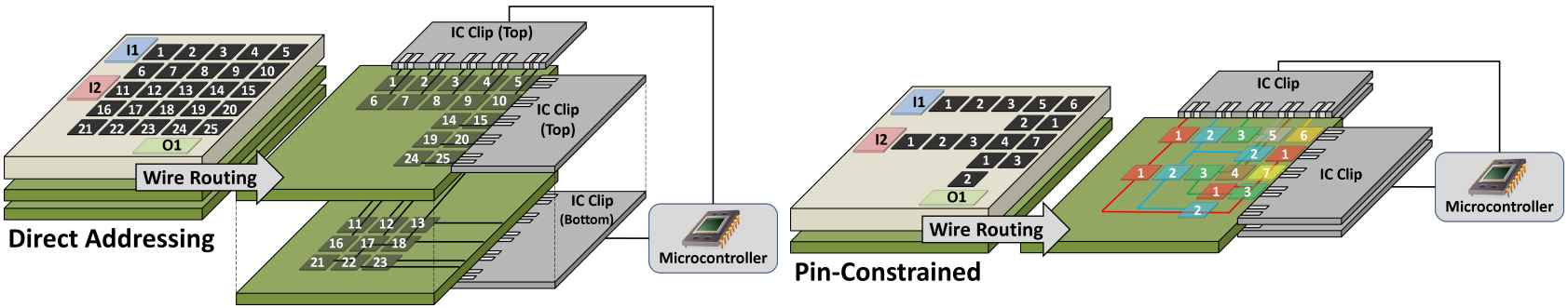
# Problem Definition




## Given

- A pin mapping of electrodes
- The size of the chip
- The wire capacity between electrodes

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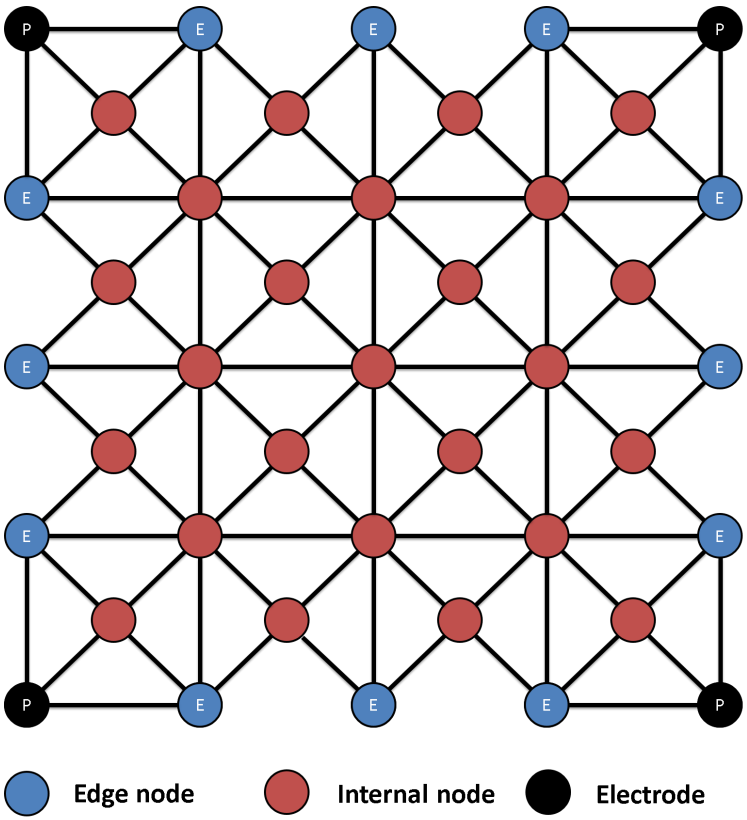
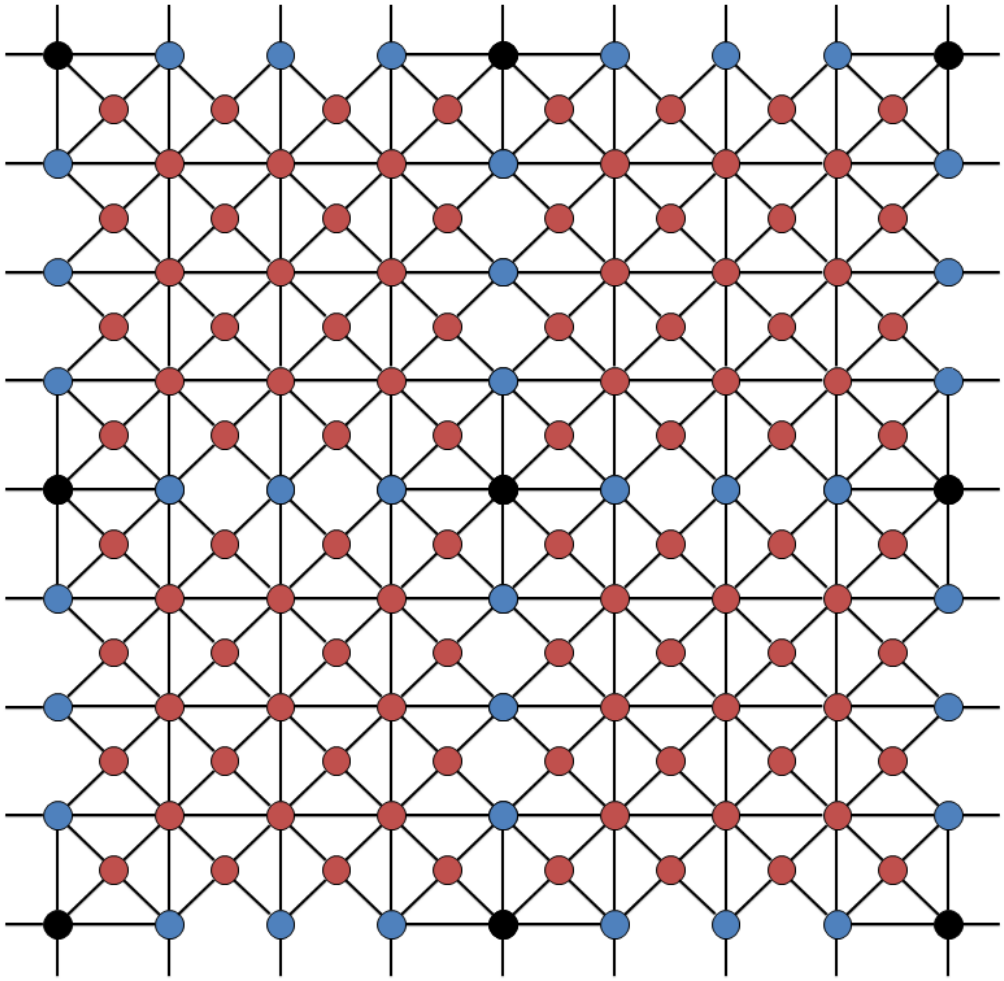
# Graph Representation




- Routing Resource Graph (RRG) for a single tile
- Wire capacity of three between electrodes

# Graph Representation Cont'd



A 2x3 grid of tiles. Only the electrode in the middle is used.

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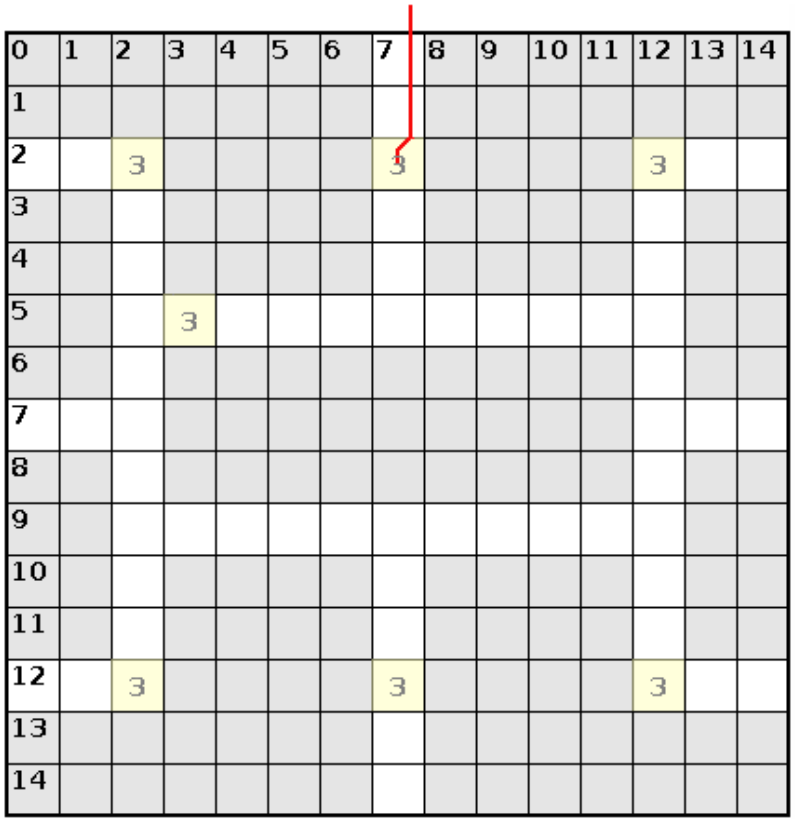
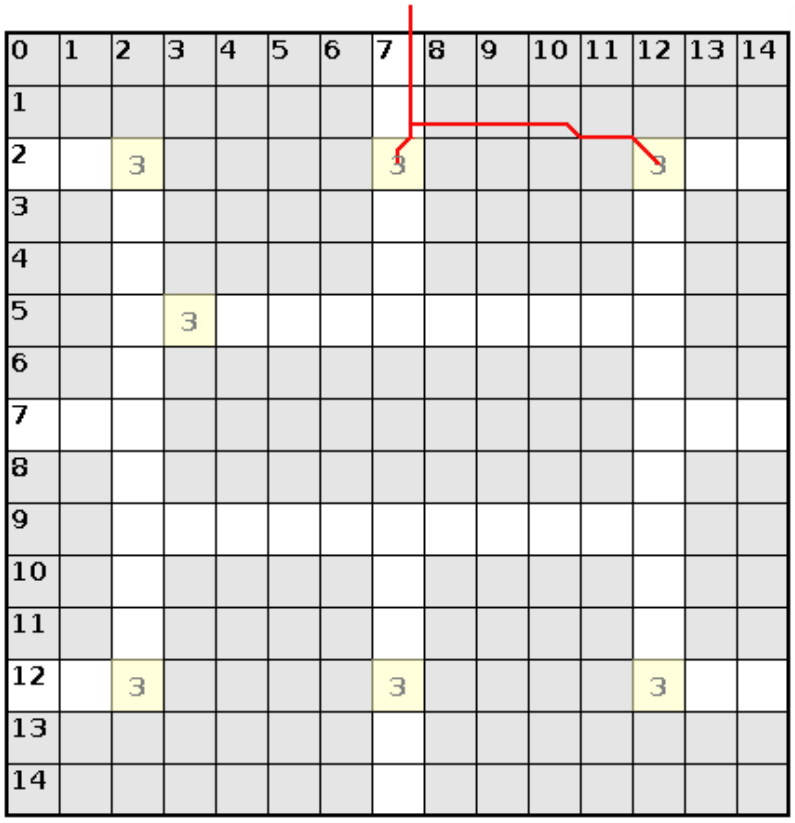
# Multi-Terminal Escape Routing



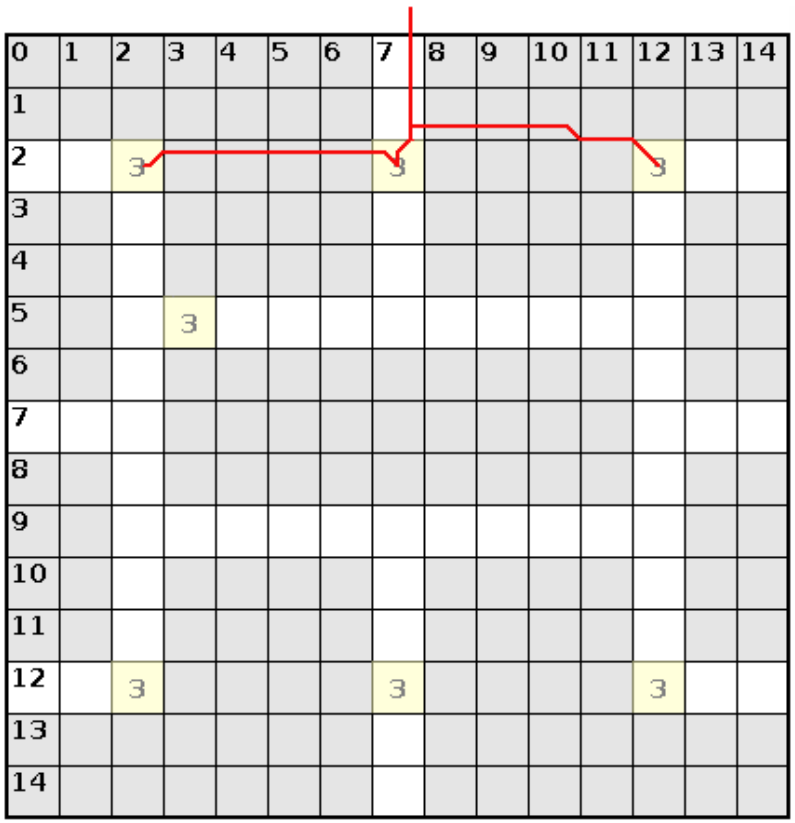

1. Super Escape node connects to every node on the edge
2. Route from Super Escape to first sink encountered on pin group

# Multi-Terminal Escape Routing Cont'd



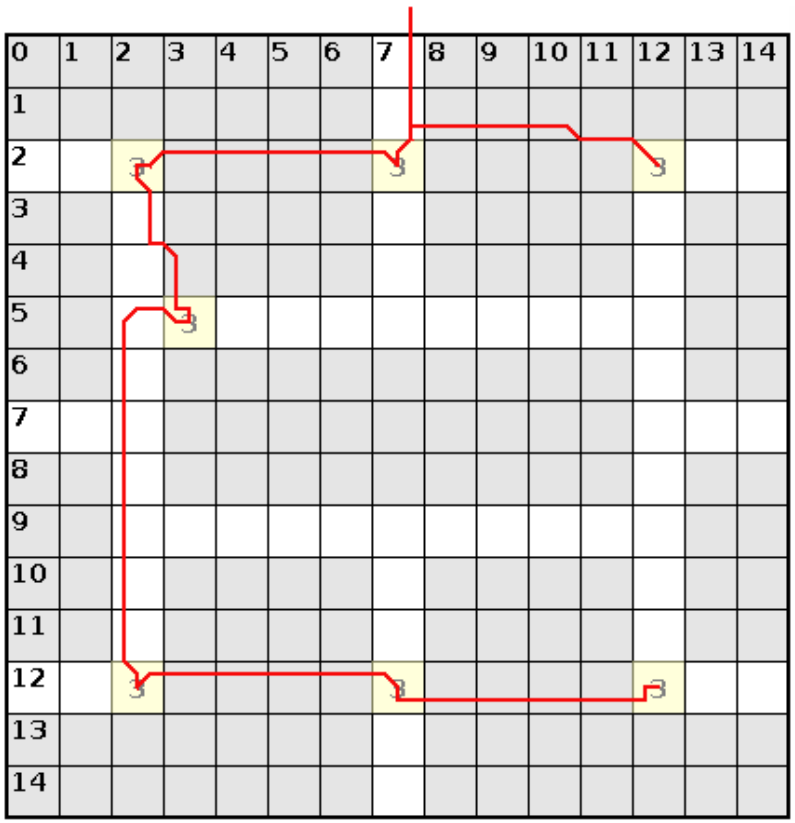

3. Route from existing path to next sink encountered on pin group

# Multi-Terminal Escape Routing Cont'd




4. The process continues...

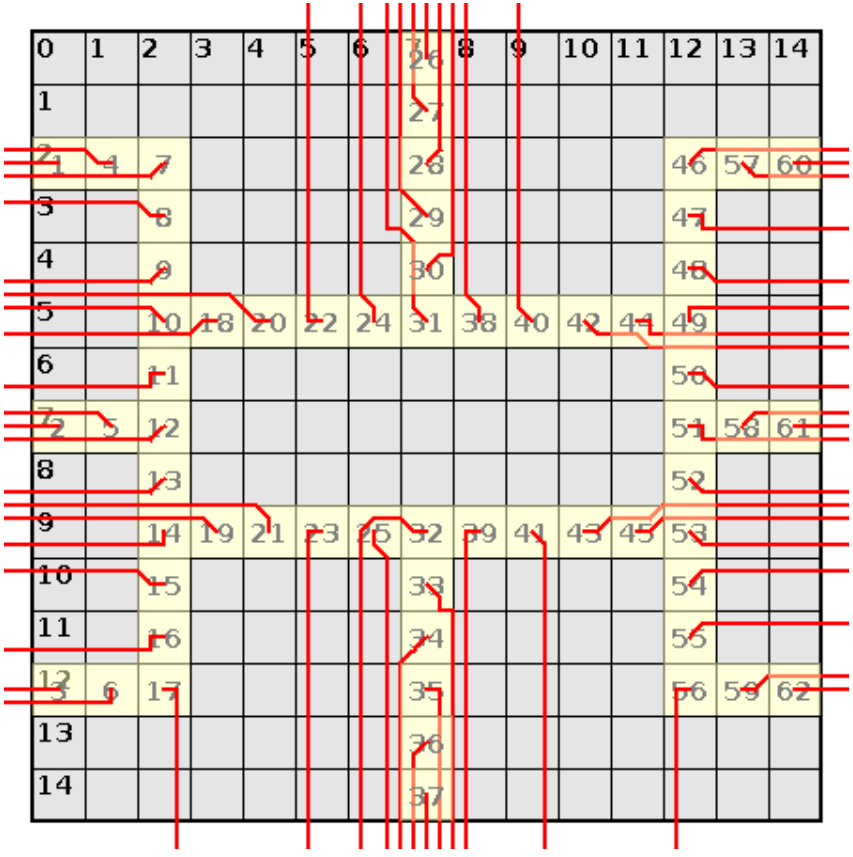
# Multi-Terminal Escape Routing Cont'd




5. until all sinks in the pin group have been found.

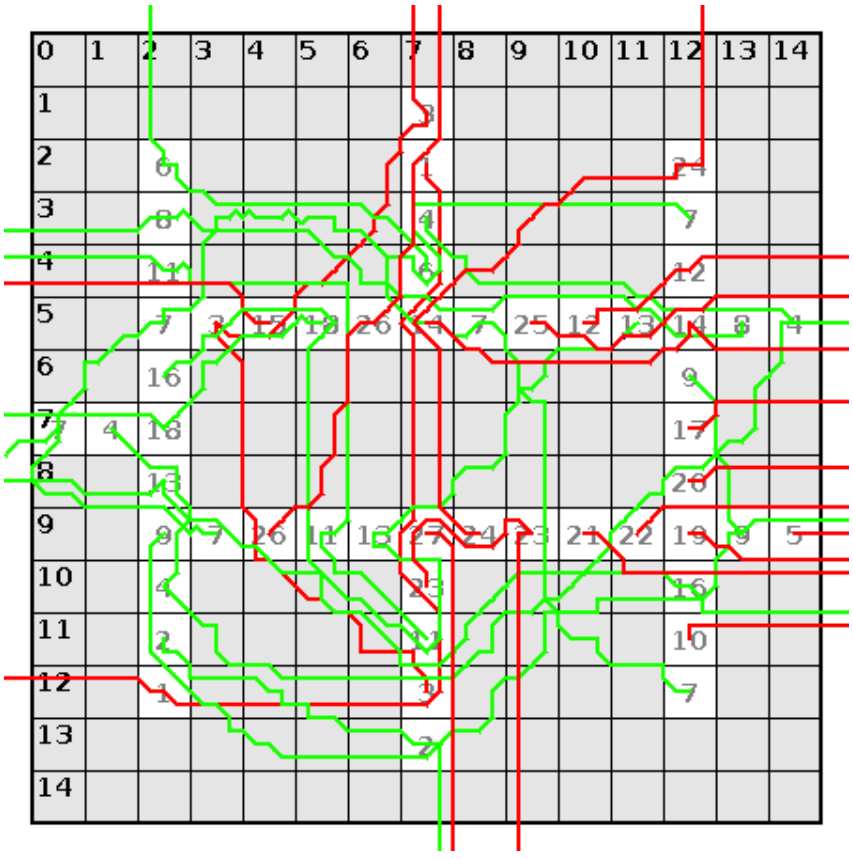
# Successful Single Layer Routing

- The direct addressed PCR chip routed successfully on a single layer.



# Failed Single Layer Routing

- The red lines indicate successfully routed pin groups.
- The green lines indicate pin groups that intersect one of the existing channels



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# Multiple PCB Layer Routing

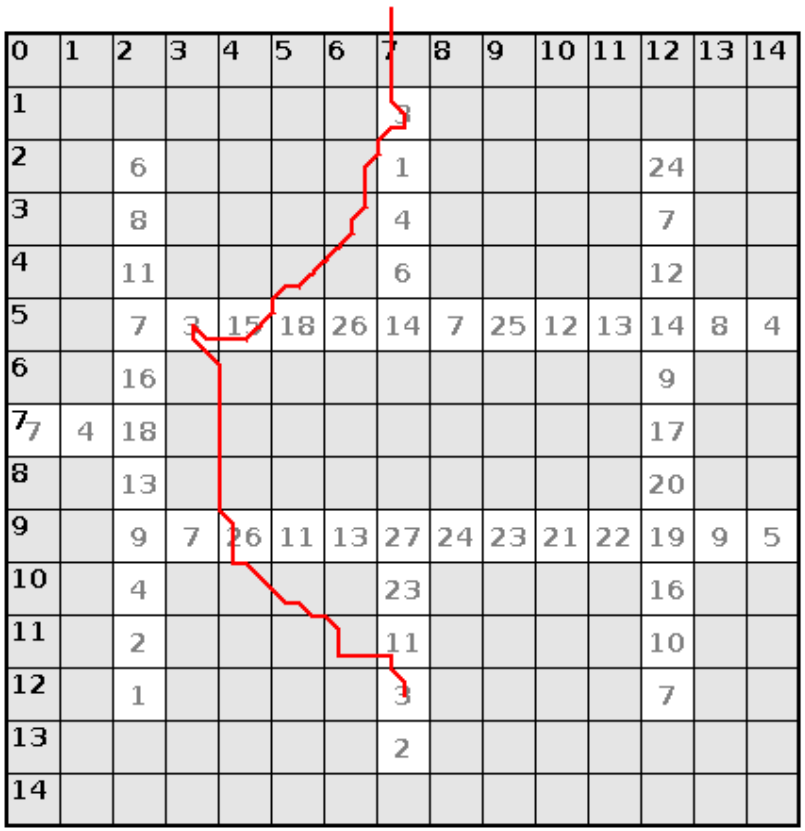
## Key Observations

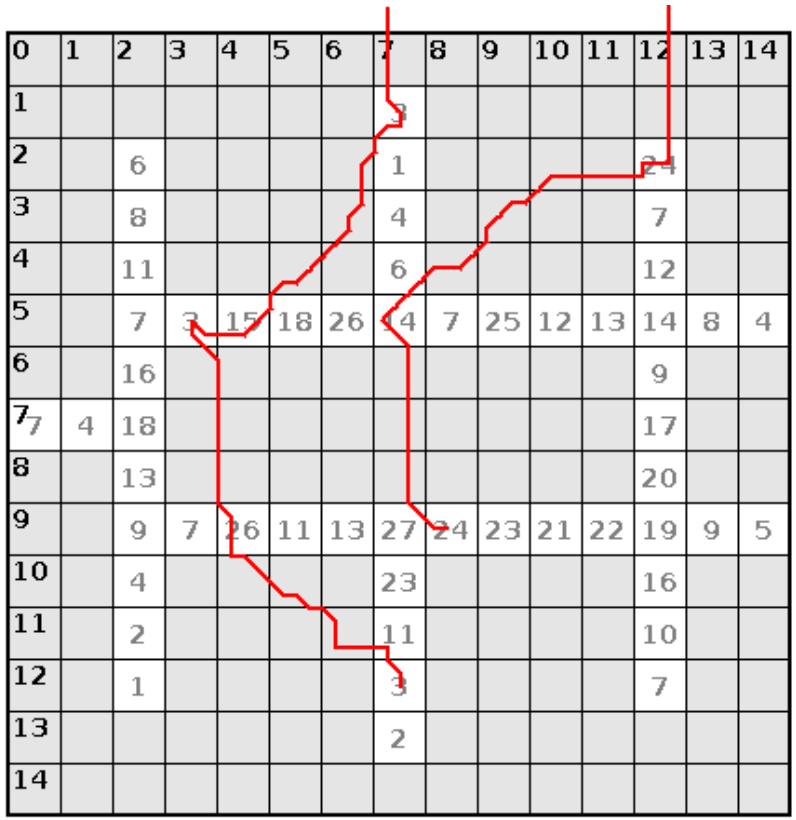
- Unable to route all chips on a single layer
- Multiple PCB layers are allowed

## General Idea

- Route as many pin groups as possible on one layer
- Push remaining pin groups to the next layer
- Repeat until all pin groups have been routed

# Multiple PCB Layer Routing Cont'd

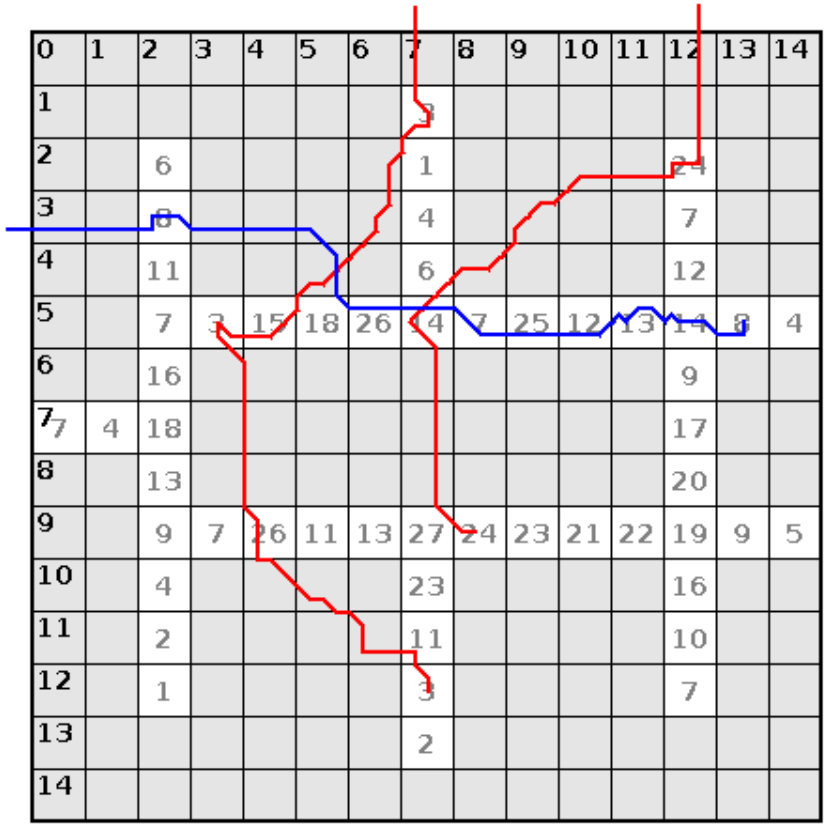



1. Route pin groups one at a time using the single layer method

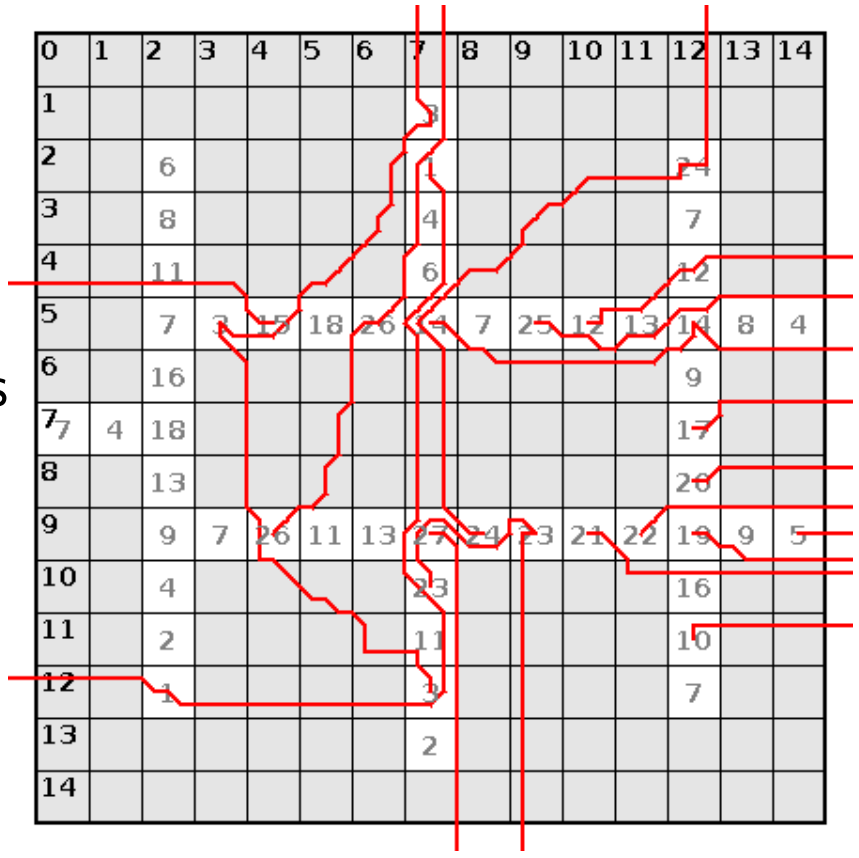
# Multiple PCB Layer Routing Cont'd

2. If current route intersects with a previous route, push it to a later layer



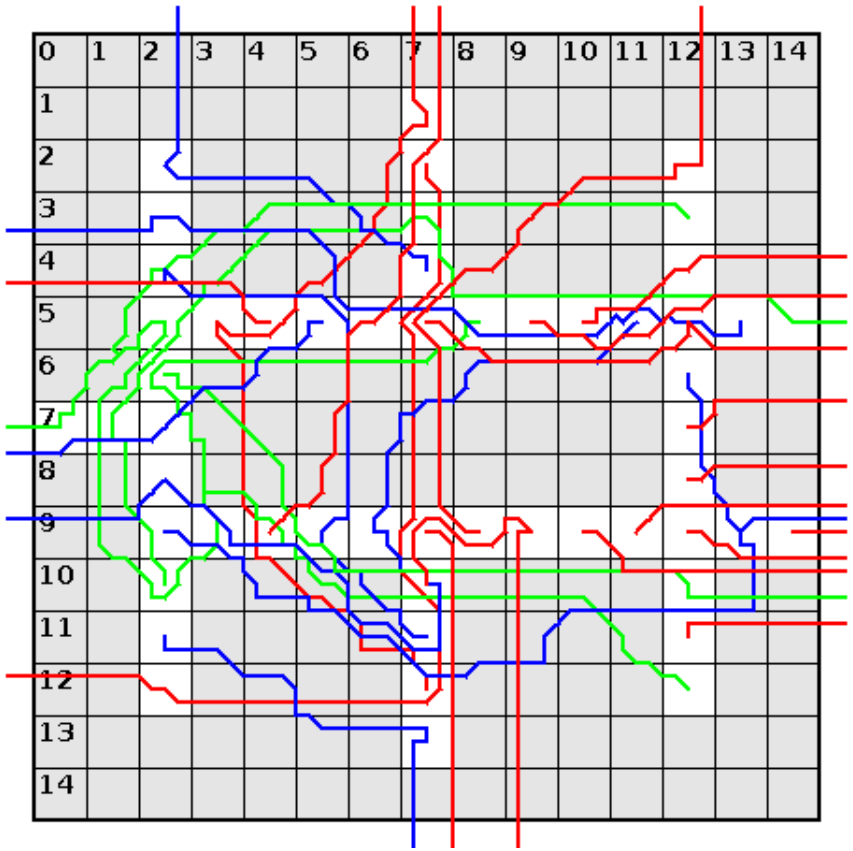
# Multiple PCB Layer Routing Cont'd

3. Route as many pin groups as possible on the current layer



# Multiple PCB Layer Routing Cont'd

4. Continue until all pin groups have been routed
   - Each color represents a separate layer.



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# Direct Addressing Results

| Benchmark | Pin | Layered Pathfinder | | [1] | |
|---|---|---|---|---|---|
| | Count | Time (s) | Layers | Time (s) | Layers |
| PCR_DA | 62 | 0.320 | 1 | 0.557 | 2 |
| Protein_DA | 54 | 0.301 | 1 | 0.597 | 2 |
| InVitro_DA | 59 | 0.335 | 1 | 0.406 | 2 |
| Multi_DA | 81 | 0.411 | 1 | 1.028 | 2 |
| IA 10x10 | 100 | 0.183 | 1 | 0.363 | 2 |
| IA 15x15 | 225 | 32.842 | 1 | 3.936 | 2 |
| IA 15x19 | 285 | 54.558 | 2 | 8.412 | 3 |
| IA 30x30 | 900 | 1436.7 | 5 | 219.247 | 6 |

[1] S.-H. Yeh, J.-W. Chang, T.-W. Huang, and T.-Y. Ho. Voltage-aware chip-level design for reliability-driven pin-constrained EWOD chips. *Proceedings of the International Conference on Computer-Aided Design - ICCAD '12*, 2012

# Pin Constrained Results

| Benchmark | Pin | Layered Pathfinder | | [1] | |
|---|---|---|---|---|---|
| | Count | Time (s) | Layers | Time (s) | Layers |
| Zhao_PCR | 14 | 15.338 | 4 | 2.162 | 5 |
| Luo_PCR | 22 | 18.824 | 5 | 3.401 | 6 |
| Zhao_Protein | 27 | 10.655 | 3 | 1.688 | 4 |
| Luo_Protein | 21 | 11.435 | 4 | 1.700 | 4 |
| Zhao_InVitro | 25 | 14.350 | 4 | 2.371 | 5 |
| Luo_InVitro | 21 | 16.358 | 5 | 2.278 | 5 |
| Zhao_Multi | 32 | 15.995 | 5 | 3.181 | 5 |
| Luo_Multi | 27 | 16.204 | 6 | 4.543 | 6 |
| FPPC 12x15 | 33 | 17.941 | 4 | 1.777 | 5 |

[1] S.-H. Yeh, J.-W. Chang, T.-W. Huang, and T.-Y. Ho. Voltage-aware chip-level design for reliability-driven pin-constrained EWOD chips. *Proceedings of the International Conference on Computer-Aided Design - ICCAD '12*, 2012

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# Conclusion

- Developed a Multi-Terminal Wire Routing algorithm for Digital Microfluidics based on Negotiated Congestion
- Extended the router for multiple PCB layers
- Extended existing single layer router to multiple PCB layers
- Reduced number of layers by 26.59% on average from an existing algorithm