Active-HDL Manual

Content

1. Create a design file (.vhdl) .................................................................2
   1.1 Set up the programming environment ..........................................2
       Step 1: Select “Create new workspace” ......................................2
       Step 2: Type in the workspace name and choose a proper directory (you
       may use the default one). .................................................................3
       Step 3: Select “Create an empty design”. Next time you run Active-HDL, you
       may choose “Add existing resource files” ......................................4
       Step 4: Leave everything as it is, and click on next ......................5
       Step 5: Type in the design name. Then click on “finish” to confirm ..6
       Step 6: Double click on “Add new file” on the design window to make the
       VHDL file..........................................................................................7
   1.2 Create the design with Language Assistant (entity, architecture) ........8
       Step 1: Select “Language Assistant” from “Tools” .......................8
       Step 2: Create Entities and Architectures. Just follow the information from
       the pop up window.........................................................................9
   1.3 Compile (F11) ..............................................................................9

2 Create a benchmark ............................................................................11
   2.1 Use Generate Test Bench from the Tool bar. Just follow the instructions.
       (You may simply use all the default settings.) .............................11
   2.2 Create benchmark with Language Assistant (process statement, assert).11
   2.3 Compile (F11) .............................................................................11

3 Create a new Waveform ......................................................................11
   3.1 set up for a wave form.................................................................11
   3.2 Run the simulation.......................................................................12
1. Create a design file (.vhdl)

1.1 Set up the programming environment

Step 1: Select “Create new workspace”
Step 2: Type in the workspace name and choose a proper directory (you may use the default one).
Step 3: Select “Create an empty design”. Next time you run Active-HDL, you may choose “Add existing resource files”
Step 4: Leave everything as it is, and click on next
Step 5: Type in the design name. Then click on “finish” to confirm.
Step 6: Double click on “Add new file” on the design window to make the VHDL file.

So far, we have finished everything we need before starting the design.
1.2 Create the design with Language Assistant (entity, architecture)

Step 1: Select “Language Assistant” from “Tools”
Step 2: Create Entities and Architectures. Just follow the information from the pop up window.

1.3 Compile (F11)

Once you have done with all the coding, you may start to compile. Click on F11 or right-click on the file name appearing on the design window. If an error is confronted during the compilation, a red line will be shown underneath the problematic line in the source code. Otherwise, you will find **GREEN** success information in the command window at the bottom of the page.
```vhdl
architecture BEHAVIORAL of A16 is
begin
  process
  variable gcd2: std_logic_vector(7 downto 0);
  begin
    if num1 > num2 then
      num1 <= num1 - num2;
      gcd2(7) := '1';
      gcd2(6) := '0';
    else
      num2 <= num2 - num1;
      gcd2(7) := '0';
      gcd2(6) := '1';
    end if;
    if num1 = 0 then
      gcd <= num2;
    end if;
    wait;
  end process;
end;
```

2 Create a benchmark

2.1 Use Generate Test Bench from the Tool bar. Just follow the instructions. (You may simply use all the default settings.)

2.2 Create benchmark with Language Assistant (process statement, assert)

2.3 Compile (F11)

Step b and c are the same as what we did when create a design file. Use that part as reference. After this step, we will have a test bench for our original file. Later on, we are going to verify the code with wave forms. See if the test bench runs correctly with our code.

3 Create a new Waveform

3.1 set up for a wave form

Click on “New WaveForm” from the tool bar. Then select “Structure” sheet at the bottom of the Design Browser to change a different view, in which we will find all the signals. After that, click on the test bench name, and select all the variables (input and output) and drag them to the wave form window
3.2 Run the simulation
Click on F5 to start the simulation. Check all the wave forms for the cases you’ve listed in the test bench. Modify the design file if there is something wrong.